INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO FORM 1449	Atty. Docket No. 2207/10554	Serial No. To Be Assigned
	Applicant(s) Hoskote et al.	
	Filing Date Herewith	Group To Be Assigned

U. S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE
	5,638,381	Jun. 10, 1997	Cho et al.			
	6,141,633	Oct. 31, 2000	Iwashita et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION	
						YES	NO

OTHER DOCUMENTS

EXAMINER'S INITIALS		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Hulgaard et al., *Equivalence Checking of Combinational Circuits Using Boolean Expression Diagrams*, Danish Technical Research Council.
		Cornelis A.J. van Eijk, *Formal Methods for the Verification of Digital Circuits*, dissertation dated Sept. 9, 1997, Eindhoven University of Technology, Netherlands, pgs. 1-144

EXAMINER	DATE CONSIDERED
	6/24/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.